REMARKS

Claims 1-35 are pending in the application. Claims 1-13 are withdrawn from consideration. Election of claims 14-28 is acknowledged. Claims 14-28 are rejected. Claims 14, 18, 22 and 26 are rejected under 35 USC § 112. Claims 14-16, 18-20, 22-14 and 26-27 are rejected under 35 USC 102(e) as being anticipated by U.S. Pat. No. 5,923,969 to Oyamatsu ("Oyamatsu"). Claims 14-16, 18-20, 22-24, 26-27 and 17, 21, 25, 28 are rejected under 35 USC 103(a) as being unpatentable over Oyamatsu in view of U.S. Pat. No. 6,020,616 to Bothra et al ("Bothra") or Japanese Pat. No. 9-289251 ("Japanese '251").

Brief Description of the Drawings

FIGS 6-9 and 13-16 are not mentioned individually in the Brief Description of the Drawings of the Specification. This has been corrected.

Abstract

The abstract has been corrected to describe the device layout to which the claims are directed.

Claim Rejections - 35 USC § 112

Claims 14, 18, 22 and 26 are rejected under 35 USC § 112. Claims 14, 18, 22 and 26 have been amended to clarify that active regions have electrodes disposed on the substrate, that the gates are disposed between the electrodes, and which gap is being referred to. Claims 18 and 22 have been amended to contain sufficient antecedent basis for the limitation "the transistors gates."

Claim Rejections - 35 USC § 102(e)

Claims 14-16, 18-20, 22-24 and 26-27 are rejected under 35 USC 102(e) as being anticipated by U.S. Pat. No.5,923,969 to Oyamatsu.

Oyamatsu does not teach claims 14-16, 18-20, 22-24 and 26-27. Oyamatsu teaches gates and dummy gates which are temporarily formed. Col. 3, lines 48-49. Applicant's invention contains no reference to the temporary formation of gates and dummy gates.

It has also been stated that Oyamatsu teaches gates of a substantially constant gap and dummy gates of substantially the same gap. Oyamatsu in fact teaches the opposite.

> If the gate-to-gate distance in a case where no contact is disposed is set to Smin and the gate-to-gate distance in a case where a contact is disposed is

set to a value (2Smin + Lmin) obtained by adding the minimum gate dimension Lmin to a value which is twice the gate-to-gate distance Smin set in a case where no contact is disposed. . .

Col. 11, lines 34-39. Oyamatsu teaches that gates containing contacts are larger in size than gates without contacts. In no way can it be argued that this teaches gates and dummy gates of substantially constant or identical gaps.

Claim Rejections - 35 USC § 103(a)

Claims 14-16, 18-20, 22-24, 26-27 and 17, 21, 25, 28 are rejected under 35 USC 103(a) as being unpatentable over Oyamatsu in view of Bothra et al or Japanese '251. As previously stated, Oyamatsu does not teach transistor gates or dummy gates of substantially constant or identical gap. Therefore, together Oyamatsu and Bothra do not make Applicant's invention obvious.

Claims 29-39 have been added to further distinguish the invention over the art of record. Support for these claims appears in Figures 11-17 and the related specification text.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 14-35 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

Page 2, line 17 and ending at page 2, line 24:

As shown in Fig. 2, etching of the oxide layer through open regions of photo resist 16 produces undercut of silicon dioxide 12, as described by circles that increase in radius to the depth of silicon 10. The greater the radius of the circle, the more deeply the photo resist 16 gets undercut. The extent to which the photo resist 16 may be undercut cannot be known until the photo resist 16 is removed. But the shape of the edge of the oxide layer pattern (as shown with dot lines in Fig. 2) is a good indicator of the degree of undercut. In other words, the etching process is not uniform thereby producing undesirable process deviations. These etching process deviation also vary widely between gates having irregular gaps there between [therebetween].

Page 4, line 25 and ending at page 4, line 26:

Fig. 5 illustrates the layout of sources, drains and gates of the transistors which make up the sense amplifier.

Fig. 6 illustrates contacts formed in the layout shown in Fig. 5.

Fig. 7 illustrates metals formed at the contacts shown in Fig. 6.

Fig. 8 illustrates contacts formed at the metals shown in Fig. 7.

Fig. 9 illustrates metal lines formed along with the contacts shown in Fig. 8.

Fig. 10 illustrates metals for applying power voltage and grounding voltage to the metal lines.

Page 5, line 3 and ending at page 5, line 4:

Fig. 12 illustrates a layout method of the sense amplifier as shown in Fig. 4 in accordance with an embodiment of the present invention.

Fig. 13 illustrates contacts formed in the layout shown in Fig. 12.

Fig. 14 illustrates metals formed at the contacts shown in Fig. 13.

Fig. 15 illustrates contacts formed at the metals shown in Fig. 14.

Fig. 16 illustrates metal lines formed along with the contacts shown in Fig. 15.

Page 5, line 18 and ending at page 5, line 22:

However, there is a problem in the conventional layout method of neighboring circuits of the semiconductor device in that the transistor gates of the neighboring circuits

have been arranged at an irregular gap in the conventional layout method of the semiconductor device, thereby increasing [a] variances in process deviations at the transistor gates in the course of the photo and etching processes.

In the Abstract

A [layout method of a] semiconductor device layout [comprising the steps of] involving the following: arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate; arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a constant gap on the substrate; and arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors (or between and outside transistors) at the same gap as that of the gates of transistors on the substrate, so that all the gates of transistors are arranged at a constant gap to minimize the variance of process deviations and accordingly reduce the difference of threshold voltage of transistors, thereby increasing reliability of the semiconductor device.

In the Claims

14. (Amended) A semiconductor device comprising:

a substrate;

active regions of [a plurality of] two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates [of transistors] disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially [constant] identical gap between ones of the adjacent transistor gates on the substrate; and

a plurality of dummy gates having predetermined width and length between [a plurality of] ones of the adjacent transistors at a substantially identical [the same] gap between adjacent ones of the dummy gates as that [of] between the adjacent ones of the transistor gates [of transistors] on the substrate.

15. (Amended) The device, as defined in claim 14, wherein the length of the dummy gates is substantially the same as that of the transistor gates [of the transistors].

18. (Amended) A semiconductor device comprising:

a substrate;

active regions of [a plurality of] two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates [of transistors] disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially [constant] identical gap between adjacent ones of the transistor gates on the substrate; and

a plurality of dummy gates having predetermined width and length between and outside [a plurality of] ones of the adjacent transistors at a substantially [the same] identical gap between adjacent ones of the dummy gates as that [of] between the adjacent ones of transistor gates [of transistors] on the substrate.

19. (Amended) The device, as defined in claim 18, wherein the length of the dummy gates is substantially the same as that of the transistor gates [of the transistors].

22. (Amended) A semiconductor device comprising:

a substrate;

active regions of [a plurality of] two or more adjacent transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of [gates of] transistor[s] gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially [constant] identical gap between ones of the adjacent gates on the substrate; and

a plurality of dummy gates having predetermined width and length outside [a plurality of] ones of the adjacent transistors at a substantially [the same] identical gap between adjacent ones of the dummy gates as that [of] between the adjacent ones of the transistor gates on the substrate.

Claims 26-28 are cancelled.

29. (New) A semiconductor device comprising:

a substrate;

active regions having a source region and a drain region on the substrate;

a portion other than the active region on the substrate;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent gates;

a plurality of dummy gates formed on the portion, the dummy gates being characterized by a second gap between adjacent dummy gates;

wherein the second gap is substantially identical to the first gap.

30. (New) The device, according to claim 29, in which a first metal is connected to the source region and the drain region by a plurality of contacts.

31. (New) The device, according to claim 30, in which a second metal is connected to a first part of the first metal to supply a voltage.

32. (New) The device, according to claim 31, in which the plurality of dummy gates are commonly connected by a second part of the first metal to supply a ground voltage.

33. (New) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region [respectively] and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first gates being characterized by a first gap between neighboring transistor gates;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second gates also being characterized by the first gap between neighboring gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring dummy gates;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring dummy gates;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

34. (New) The semiconductor device according to claim 33, in which the first gap is substantially identical to the second gap.

35. (New) The semiconductor device according to claim 33, in which the second metal is connected to a second part of the first metal to supply a ground voltage.

36. (New) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions, the plurality of transistor gates being characterized by a predetermined first dimension and a variable second dimension on the substrate; and

a plurality of dummy gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, the plurality of dummy gates being characterized by dummy gates that substantially fill the region on the substrate devoid of transistor gates in the second dimension;

wherein the plurality of transistor gates have substantially identical first and second dimensions.

37. (New) The semiconductor device according to claim 36, in which the first dimension characterizes a transistor gate length.

38. (New) The semiconductor device according to claim 37, in which the second dimension characterizes a transistor gate width.

39. (New) The semiconductor device according to claim 38, in which adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.